Attorney's Docket No. TN319   **Serial No. 10/603,407**
<u>**Supplemental Amendment**</u>   <u>02/03/05</u>

Paragraphs being modified are listed below.

The first paragraph under the sub-heading Related Applications is amended as follows:

This patent is related to two other ~~patents~~ <u>currently pending patent applications</u> filed on even date herewith entitled BUILDING AND TESTING COMPLEX COMPUTER PRODUCTS WITH CONTRACT MANUFACTURERS WITHOUT SUPPLYING PROPRIETARY INFORMATION, <u>Serial No. 10/603,446,</u> and TEST APPARATUS TO FACILITATE BUILDING AND TESTING COMPLEX COMPUTER PRODUCTS WITH CONTRACT MANUFACTURERS WITHOUT PROPRIETARY INFORMATION, <u>Serial No. 10/603,900.</u>~~,~~ <u>They are related</u> in that they have substantially similar disclosure and in that all three <u>applications</u> claim priority from the same provisional application~~;~~ <u>Serial No. 60/440,724, filed 1/17/2003, now abandoned in favor of these applications</u>.

The paragraph bridging pages 9 and 10 is amended as follows:

This patent also describes various unique features of our "edge" tester and testing processes including a bar code scanner for determining which board is being applied to the tester and a safe insertion and connection process by which the tester prevents mishandling and misinsertion of boards under test. We also describe how TCL language file may be converted to a SVF file for use by the JTAG Technologies boundary scan software without revealing the proprietary information available by inspection of the TCL code file. (TCL is an internationally recognized software language with a detailed description available at several freeware locations on the internet~~, one URL is: http://www.tel.tk/~~ . Alternative languages could be used such as the currently popular C# language commonly used by Microsoft). (SVF is an acronym for a hardware description language codified in IEEE standard 1149.1 instructions. A document, currently at a Texas Instruments website (noted in

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an accompanying information disclosure for this patent): which describes SVF on page 47 et

seq and provides useful background on HSDL, 1149.1 and related topics). By providing only

a low level language file, useful descriptive information about the circuitry the assembler has

when he received this file is not revealed.

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